PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-303412
(43)Date of publication of application : 13.11.1998

(51)Int.Cl. **H01L 29/78**
H01L 21/336
H01L 21/285
H01L 21/8238
H01L 27/092

(21)Application number : 09-105000
(22)Date of filing : 22.04.1997

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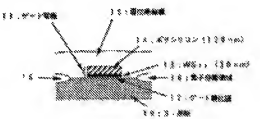
(54) SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device and a fabrication method thereof in which the gate electrode can be made thick enough to block implantation of ions into a channel when a self-aligned diffusion layer is formed by ion implantation even if a material having a work function close to the midgap of silicon is employed in the gate electrode and an undue tensile stress is not applied to a gate oxide.
SOLUTION: A gate electrode 11 is composed of WSix 13 and polysilicon 14 and the lower layer of WSix touches a gate oxide 12. Since the work function of WSix is close to the midgap of silicon, threshold voltage Vth can be controlled to a correct level. Tensile stress being applied to the gate oxide can be lessened by making thin the WSix layer and the entire gate electrode can be made thick enough by depositing polysilicon on the WSix.



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a semiconductor device and a manufacturing method for the same. In detail, a semiconductor device which can stop small the tensile stress which controls the work function of the gate electrode of the interface which touches gate oxide near [mid gap] silicon, and is added to gate oxide, and a manufacturing method for the same are started by making a gate electrode into a specific structure.
[0002]
[Description of the Prior Art]There is a thing of SOI (Silicon On Insulator) structure other than the so-called thing of bulk structure in the complementary MOS (CMOS) transistor. There is an advantage -- as for SOI structure, control of a soft error and control of latchup peculiar to a CMOS transistor are achieved easily [the complete isolation of elements]. For this reason, the trial which attains improvement in the speed and high-reliability-ization from a comparatively early stage about CMOS transistor LSI of the SOI structure which set silicon activity layer thickness to about 500 nm has been made.
[0003]In recent years, silicon layer thickness of the surface of SOI structure is made thin to about 100 nm, and channel impurity concentration is also controlled comparatively lowness, and what is called perfect depletion type CMOS of the silicon active layer the wholewas [depletion-] made toize mostly has appeared. If CMOS is used as such a perfect depletion type, it will have become clear that the outstanding performance -- control of a short channel effect and improvement in the current driving capacity of a MOS transistor are achieved -- is obtained.
[0004]By the way, in the usual enhancement type MOS transistor, in order to hold down the power consumption of the whole integrated circuit containing many transistors, there is a request of liking to make the drain current in zero bias (state of OFF) as small as possible. For

the purpose, it is necessary to make threshold voltage V_{th} to some extent high. On the other hand, the value which lengthened threshold voltage V_{th} from power supply voltage is added effective in drain sauce among the power supply voltage applied between the drain sauce of a MOS transistor. For this reason, it is inefficient when threshold voltage V_{th} is made high too much. Therefore, it is supposed that it is the appropriate value of threshold voltage V_{th} about 0.5-1.0V. However, the n^+ polysilicon used abundantly from the former for the Reason for often bearing mainly to a high temperature process, When using as a gate electrode material of CMOS, in order to make threshold voltage V_{th} of a nMOS transistor into the above-mentioned appropriate range, It becomes difficult to have to carry out impurity concentration of a channel abbreviation 10^{17} / beyond a cm^3 grade, therefore to use the MOS transistor of SOI structure as a perfect depletion type.

[0005]For this reason, using p^+ polysilicon (B-DOPOS) for a gate electrode material is examined as a method of creating the MOS transistor of an enhancement type with a perfect depletion type. However, for example, if p^+ polysilicon is used for a gate to the transistor of nMOS, Threshold voltage V_{th} is about 1.0v in the case where a channel is non-doped, and in order to lower V_{th} from this, the counter dope of doping phosphorus (P) to the channel of nMOS must be performed. However, since this counter dope increases a short channel effect, it is not preferred for the minuteness making of LSI.

[0006]Therefore, after all, also when making which of n^+ polysilicon and p^+ polysilicon into a gate electrode, an active layer is unable to control threshold V_{th} of a transistor to an about [0.5V] proper value to the thin-film-ized detailed SOI device. Since drain leak current is made increased, it is not preferred too to raise the impurity concentration of a channel in vain also to a partial depletion type transistor.

[0007]On the other hand, also in the MOS transistor by the bulk silicon which minuteness making follows, n^+ type polysilicon has been used as a material of a gate electrode. This is because the channel profile else [of often bearing to the above-mentioned high temperature process] embeds, and it becomes a mold, so mobility becomes high and can accelerate device operation. However, the MOS transistor of a buried channel has the problem of becoming easy to produce a punch through according to a short channel effect as minuteness making progresses.

[0008]About CMOS, it is required further that the absolute value of the threshold voltage of nMOS and the threshold voltage of pMOS should be made equal, i.e., symmetrize threshold voltage. In conventional CMOS, the n^+ type polysilicon film was used for any gate electrode of

nMOS and pMOS for the above-mentioned Reason. In this case, since threshold voltage V_{th} of nMOS and pMOS becomes unsymmetrical, in order to symmetrize V_{th}, the ion implantation of the boron (B) was shallowly carried out to the channel regions of pMOS, and threshold voltage V_{th} of both transistors is usually set as them almost equally. However, since the impurity concentration of a substrate face rises and carrier mobility falls by this ion implantation, it becomes disadvantageous for improvement in the speed of operation. Therefore, if only n^+ type polysilicon was used as a gate electrode, about both a nMOS transistor and a pMOS transistor, simultaneously, it is a surface channel type strong against a short channel effect, and operation cannot form a CMOS transistor [******].

[0009]For this reason, it is possible to adjust threshold voltage V_{th} not only using channel impurity concentration but using the work function of a gate electrode, To the nMOS transistor, the dual gate process using p^+ polysilicon respectively is examined to n^+ polysilicon and a pMOS transistor for this purpose. If it does in this way, threshold voltage V_{th} of both MOS transistors can also be symmetrized. A symposium one VLSI Technology (1994) abstract collection and the subject number 2.2 can be referred to for this, for example.

[0010]However, if the polysilicon in which the types of a dopant differ is used as a gate electrode by the nMOS transistor and a pMOS transistor, Since the impurity in each gate electrode is mutually spread in the portion which the n^+ polysilicon gate of nMOS and the p^+ polysilicon gate of pMOS connect, There is a problem of changing the work function of each gate electrode sharply, and also changing threshold voltage V_{th} sharply for this reason. This problem becomes remarkable especially, when silicide, such as tungsten silicide (WSi_x), is used for the upper layer of polysilicon for low-resistance-izing of a gate electrode.

[0011]Drawing 14 is a figure for explaining this.

If the nMOS transistor 50 (the polysilicon 51 of a gate electrode lower layer is a n type) at the upper left of [the] a figure and the pMOS transistor 52 (the polysilicon 53 of a gate electrode lower layer is a p type) at the upper right of [the] a figure are contacted and CMOS54 of the said figure bottom is formed, Since the dopant of a different type included in polysilicon of a gate electrode lower layer of each transistor is mutually spread through the upper tungsten silicide layers 55 and 56, the work function of the polysilicon 51 and 53 is changed.

This is because the diffusion coefficient of the dopant in silicide is dramatically large.

[0012]From this, the polysilicon in which the types of a dopant differ in the gate electrode of both transistors too is not used in the CMOS device by bulk silicon, Using the gate electrode same type which has a work function near [central (mid gap)] the band gap of silicon is examined. High-melting point metal silicide with what [near / mid gap / silicon / much /

specifically] has a work function attracts attention as a gate electrode material, Especially, since neither molybdenum silicide ($MoSi_x$) nor tungsten silicide (WSi_x) carries out a direct reaction to SiO_2, it does not degrade gate pressure-proofing greatly and attracts attention especially as a gate electrode material. Drawing 15 is an example of the MOS transistor which used the tungsten silicide (WSi_x) 60 as a gate electrode of a monolayer. In this case, although only one MOS transistor is illustrated, the tungsten silicide of the same monolayer also as the MOS transistor of another side which constitutes CMOS is used as a gate electrode.

[0013]

[Problem(s) to be Solved by the Invention]By the way, a gate electrode plays the important role of preventing ion being poured into the channel directly under a gate electrode, when forming the diffusion zone (henceforth "sauce/drain diffused layer") of sauce and a drain by the ion implantation by self align. For this reason, it is necessary to make a gate electrode into the thickness for which self align is enough to form a diffusion zone. It is required to also make more than into sufficient thickness, for example, 150 nm, the gate electrode of the tungsten silicide 60 shown in drawing 15 in consideration of this point.

[0014]However, high-melting point metal silicide has many which have the big internal stress of an order called 10^9Pa in after membrane formation at one side. Thus, when it forms as a gate electrode by the thickness of the grade which can form the diffusion zone according material with big internal stress to self align, a big tensile stress will be impressed to the gate oxide of a ground. As a result, the problem that leakage current and phase boundary charge by the tensile stress added to gate oxide increase will arise, and it will lead to the reliability deterioration of the whole integrated circuit.

[0015]This invention is made based on the above-mentioned situation, and is a thing.

the purpose, even when the material which is alike and has a work function near the mid gap of silicon is used, It is providing a semiconductor device which a gate electrode's can be thickened and does not apply a superfluous tensile stress to gate oxide, and a manufacturing method for the same to such an extent that it can prevent that the ion at the time of forming the self-align diffusion zone by an ion implantation is poured into a channel.

[0016]

[Means for Solving the Problem]In a semiconductor device which it has, the 1st invention for attaining the above-mentioned purpose a gate electrode formed via gate oxide on a channel said gate electrode, A lower layer which touches said gate oxide is characterized by high-melting point metal silicide and the upper layer being the two-layer structure which consists of polysilicon.

[0017]In a semiconductor device with which the 2nd invention for attaining the above-

mentioned purpose has the gate electrode formed via gate oxide on a channel, Said gate electrode was made into three layer systems which high-melting point metal silicide becomes in a lower layer which touches said gate oxide, and metal nitride and the upper layer become from polysilicon in a middle lamella. In a semiconductor device which the 3rd invention for attaining the above-mentioned purpose has the gate electrode formed via gate oxide on a channel, and has a LDD layer to both ends of a channel, A lower layer which touches said gate oxide said gate electrode High-melting point metal silicide, It has a sidewall for preventing pouring of impurity ion to said LDD layer at the time of forming the sauce/drain diffused layer which the upper layer is the two-layer structure which consists of polysilicon, and was formed in the side of said gate electrode.

[0018]This invention is characterized by a manufacturing method of a semiconductor device which is the 4th invention comprising the following, in order to attain the above-mentioned purpose.

A process of forming a refractory metal silicide film via gate oxide on a channel.

A process of forming a polysilicon film on said refractory metal silicide film.

A process of forming a gate electrode which consists of high-melting point metal silicide and polysilicon which etched said refractory metal silicide film and a polysilicon film, and were patternized by specified shape.

A process of pouring in impurity ion and forming sauce/drain diffused layer.

[0019]High-melting point metal silicide can be chosen from among tungsten silicide (WSi_x), molybdenum silicide ($MoSi_x$), tantalum silicide ($TaSi_x$), and titanium silicides ($TiSi_x$) in said 1st [the] thru/or the 4th invention. As for polysilicon, any one or more of arsenic (As), phosphorus (P), and boron (B) may be doped. High-melting point metal silicide is formed with a CVD method using mixed gas containing high-melting point metal fluoride and a chlorosilicane system compound, for example.

[0020]Since the 1st invention can control a work function which affects threshold voltage by making into high-melting point metal silicide a lower layer which touches gate oxide among gate electrodes near the center (mid gap) of a band gap of silicon, Threshold voltage V_{th} is controllable to a proper value. By forming comparatively small polysilicon of internal stress on this high-melting point metal silicide, It can make to pour in impurity ion unnecessary for a channel part in thickness of the whole gate electrode in the case of the sauce / drain diffusion stratification by self align into sufficient thickness to prevent. Since thickness of high-melting point metal silicide with large internal stress can be formed in sufficient thinness, a tensile stress impressed to gate oxide becomes small.

[0021]The 2nd invention by having made a gate electrode into three layer systems which a

lower layer calls high-melting point metal silicide, a middle lamella calls metal nitride, and the upper layer calls polysilicon, When an impurity is further introduced and conductor-ized to the upper polysilicon in addition to an operation and an effect of the 1st invention, since it can prevent that the impurity is spread to lower layer high-melting point metal silicide with medium-rise metal nitride, Change of a work function of lower layer high-melting point metal silicide can be suppressed effectively.

[0022]By [said] providing a sidewall more, the 3rd invention has an operation and an effect of the 1st invention, for example, can realize a MOS transistor of LDD structure. Since the 4th invention can control a work function which affects threshold voltage by making into high-melting point metal silicide a lower layer which touches gate oxide among gate electrodes near the mid gap of silicon, For example, threshold voltage V_{th} of a field effect transistor is controllable to a proper value. By forming comparatively small polysilicon of internal stress on this high-melting point metal silicide, It can make to pour in impurity ion unnecessary for a channel part in thickness of the whole gate electrode in the case of the sauce / drain diffusion stratification by self align into sufficient thickness to prevent. Since thickness of high-melting point metal silicide with large internal stress can be formed in sufficient thinness, a tensile stress impressed to gate oxide becomes small.

[0023]

[Embodiment of the Invention]With reference to Drawings, the embodiment of this invention is described below. As mentioned above, although the work function of the material used as a gate electrode affects threshold voltage V_{th} of a gate, the influence is mostly decided with the work function of the very thin portion which touches gate oxide among gate electrodes. On the other hand, the tensile stress which a gate electrode impresses to gate oxide is dependent on the internal stress and thickness of a gate electrode material. Therefore, if what has small internal stress is used as a gate electrode material, it can make to be able to make small the tensile stress impressed to gate oxide, and to pour in impurity ion unnecessary for a channel part in the case of the diffusion-zone formation by self align into the thickness of the grade which can be prevented. Paying attention to such a point, it is supposed that the high-melting point metal silicide which has a work function is used near [mid gap] silicon at the thin portion which touches gate oxide among gate electrodes, It forms even in the thickness of the grade which can prevent that impurity ion unnecessary for a channel part is poured in on it in polysilicon with small internal stress in the case of the diffusion-zone formation by self align, these both are combined, and it is considered as a gate electrode.

[0024]Drawing 1 is a sectional view showing the structure of the gate electrode of a 1st embodiment of this invention used with semiconductor devices, such as CMOS. However, since the structure of the gate electrode of drawing 1 is common by nMOS and pMOS, it has not distinguished both in particular. The MOS transistor of drawing 1 is formed on the silicon

substrate 10 of bulk state. The gate electrode 11 passes in between the gate oxide 12 which consists of SiO_2, and is formed in the upper part of the silicon substrate 10. The gate electrode 11 consists of a bilayer of the lower layer tungsten silicide (WSi_x) 13 and the upper polysilicon 14. Therefore, the tungsten silicide 13 is in contact with the gate oxide 12 among the gate electrodes 11. To the upper polysilicon 14, arsenic (As) is doped with the dose of $5x10^{15}/cm^2$, and impurity concentration is made into abbreviation $4.2x10^{20}$ / cm^3 grade. Thereby, the polysilicon 14 serves as a conductor thoroughly.

[0025]The interlayer insulation film 15 is formed in the circumference and the upper layer of the gate electrode 11. The isolation region 16 by the LOCOS process for electric separation with an adjacent element is shown in the both ends of drawing 1. In drawing 1, the sauce/drain diffused layer formed into the silicon substrate 10 of both sides of the gate electrode 11 are omitted. Also in below-mentioned drawing 2 and drawing 3, it is the same.

[0026]The thickness of polysilicon of 30 nm and the upper layer sets thickness of the lower layer tungsten silicide 13 to 150 nm in 120 nm and the sum total among the bilayers which constitute the gate electrode 11. If there is thickness of this level, it can prevent effectively that impurity ion is poured into a lower layer channel in the case of the sauce / drain diffusion stratification by self align.

[0027]the internal stress of tungsten silicide being done and coming out of it on the other hand, -- about -- it is a 10^9Pa grade and compares with it of polysilicon -- it is large about single figure. If such tungsten silicide is deposited on about 150-nm thickness, it originates in the internal stress, a very big tensile stress is impressed to the lower layer gate oxide 12, and leakage current and phase boundary charge in gate oxide increase. However, if the thickness of the tungsten silicide 13 is suppressed to about 30 nm as mentioned above, This is about 1/10 thinness of the thickness of the usual polysilicon gate, and even if it forms the 120-nm polysilicon 14 on this, it can stop the internal stress as the gate electrode 11 whole to the same extent as the case of a general polysilicon gate.

[0028]Although it is desirable in this embodiment for the thickness of the tungsten silicide 13 to be about 30 nm as mentioned above, even if it makes it thin, for example to about 10 nm, the effect that threshold voltage V_{th} of a transistor can be adjusted to a suitable value is acquired.

On the other hand, although it depends for the maximum of the thickness of the tungsten silicide 13 also on the size of permissible internal stress, and the thickness of the polysilicon 14 laminated upwards, Although suppressing to about about 100 nm is desirable and it set to about 120 nm above thickness of the polysilicon formed on the tungsten silicide 13, If the thickness of the whole gate electrode becomes thin too much, the effect which formation of the sidewall for LDD mentioned later becomes difficult, and covers the impurity ion in the case of diffusion-zone formation will also fall. It is required for the thickness of polysilicon to set to 120

nm and about at least 90 nm desirably from this viewpoint. Therefore, when the thickness of the tungsten silicide 13 is 30 nm, the thickness of the polysilicon 14 will call it the 3 or more times.

[0029]The work function of high-melting point metal silicide like tungsten silicide is located near [mid gap] silicon. Therefore, if tungsten silicide is used for the portion which touches the gate oxide 12 and the gate electrode of a MOS transistor is formed, Even if it does not introduce so a lot of impurities into channel regions, threshold voltage V_{th} of a transistor can be adjusted to an about [0.5V] suitable value. Tungsten silicide may be non-doped, may dope impurities, such as arsenic (As), phosphorus (P), and boron (B), dose $1x10^{15}$ / above cm^2, and may control the work function.

[0030]For this reason, when CMOS is constituted using this MOS transistor, there is an advantage that the threshold voltage of a nMOS transistor and a pMOS transistor can be symmetrized easily. In the conventional MOS transistor using the gate electrode by polysilicon, in order for threshold voltage V_{th} to be about 0.6 v, it was required to raise channel impurity concentration more than the order of $10^{17}/cm^3$. On the other hand, if tungsten silicide is used for the portion which touches the gate oxide 12, the non-doped state of channel impure concentration is also enough as a gate to below the order of $10^{16}/cm^3$. the part whose dispersion according [the degree of electron transfer] to an impurity decreases at this time -- it becomes large and, as a result, the current driving capacity of a MOS transistor can be heightened.

[0031]By the way, O atom in SiO_2 of gate oxide is combined as more strongly [as Si atom] than W atom in a tungsten silicide (WSi_x) film. Therefore, it is greatly related to the adhesion over the gate oxide of tungsten silicide how many joint hands of Si atom in tungsten silicide can combine with O atom in gate oxide. The general method of forming tungsten silicide is what is called a Silang reduction CVD method that uses tungsten hexafluoride (WF_6) / Silang (SiH_4) mixed stock gas, for example. However, the tungsten silicide which formed membranes on gate oxide with the Silang reduction CVD method has the problem of being very easy to exfoliate. In the tungsten silicide formed with the Silang reduction CVD method, F atom of 10^{20} / cm^3 thing order contains this, and it is usually considered because the joint hand of Si atom which should be combined with O atom of gate oxide (SiO_2) is consumed by F atom.

[0032]So, in this embodiment, the tungsten silicide which is high-melting point metal silicide is formed not with the general Silang reduction CVD method but with the CVD method using the mixed gas containing high-melting point metal fluoride and a chlorosilicane system compound. Specifically, the CVD method (it is called a "dichlorosilane reduction CVD method") using the

mixed gas containing tungsten hexafluoride (WF_6) and dichlorosilane (SiH_2Cl_2) is used. The tungsten silicide formed by the dichlorosilane reduction CVD method, Probably it originates in the crystalline merit by the height of that forming temperature, and the uptake quantity of F atom is low ($1x10^{17}$ / cm^3 grade), and, for this reason, the rate of triple figures that the effective joint hand of Si atom is consumed by F atom becomes less than the tungsten silicide by the Silang reduction CVD method.

[0033]Thus, in this embodiment, the adhesion over gate oxide can be raised by forming tungsten silicide not using the Silang reduction CVD method generally used but using a dichlorosilane reduction CVD method. and the composition ratio x of Si atom to W atom of tungsten silicide (WSi_x) -- 2.7 or more -- desirable -- as 3.0 or more -- a stoichiometric composition -- Si -- pressure-proofing of the gate oxide of the 10-nm level in thickness is also maintainable good by supposing that it is rich. And unlike sputtering membrane formation, the membrane formation by a CVD method is excellent in step coverage, and since there is also little ion irradiation damage, it can also control the resistance rise by a step part, and withstand voltage degradation of gate dielectric film.

[0034]Drawing 2 is a sectional view showing the structure of the gate electrode of a 2nd embodiment of this invention used with Integrated Circuit Sub-Division, such as CMOS. In the figure, the detailed explanation is omitted by attaching identical codes about the same portion as drawing 1. Differing from drawing 1 with the structure of drawing 2 is the point of having formed the sidewall 19 which becomes having formed stopper $SiO_2$18 on the gate electrode 11, the gate electrode 11, and a side attachment wall of stopper $SiO_2$18 from polysilicon.

[0035]The thickness of stopper $SiO_2$18 may be 150 nm, for example. Even after performing a high-concentration ion implantation for diffusion-zone formation, influence can be prevented from attaining to the impurity concentration in the gate electrode 11 also to any of nMOS and pMOS by forming SiO_2 of thickness of this level on the gate electrode 11. Thereby, the type and concentration of an impurity in the tungsten silicide 13 can be maintained uniformly, and, as a result, a work function is also kept constant. Tungsten silicide may be non-doped and the point which may dope impurities, such as arsenic (As), phosphorus (P), and boron (B), dose $1x10^{15}$ / above cm^2, and may control the work function is the same as that of the case of a 1st embodiment.

[0036]The sidewall 19 plays a role of a LDD (Lightly Doped Drain) spacer. That is, when the sidewall 19 performs the ion implantation of a diffusion zone, it prevents an excessive impurity from being injected into a LDD layer. The characteristic to be oxidized improves like the after-mentioned, and even if a gate electrode is exposed to an oxidizing atmosphere as a result, it is effective in the ability to prevent the catastrophic oxidation of tungsten silicide. The thickness of

the sidewall 19 shall be about 150 nm, for example. When performing the ion implantation for diffusion-zone formation, in order to prevent channeling, it is necessary to form the oxide film (not shown) by oxidation of HTO (High Temperature Oxide) and a Si substrate with usually sufficient step coverage. By forming the sidewall 19, when forming these films, there is an advantage that tungsten silicide can be prevented from oxidizing.

[0037]Drawing 3 is a sectional view showing the structure of the gate electrode of a 3rd embodiment of this invention used with Integrated Circuit Sub-Division, such as CMOS. In the figure, the detailed explanation is omitted by attaching identical codes about the same portion as drawing 1 and drawing 2. Differing from drawing 1 with the structure of drawing 3 is the point of having formed the thin tungsten nitride (WN_x) film 20 in the interface of the tungsten silicide 13 and the polysilicon 14. The thickness of the tungsten nitride film 20 is about 3 nm. The purpose of forming the tungsten nitride film 20 is to prevent the impurity in the polysilicon 14 from being spread to the tungsten silicide 13.

[0038]The tungsten silicide 12 may be non-doped, and it dopes impurities, such as arsenic (As) and phosphorus (P), with the dose for example, about $10^{15}/cm^2$, and it may be made to control the work function to a suitable value. Since stopper $SiO_2$18 like drawing 2 does not form with the structure of this embodiment, even if it does not dope an impurity beforehand, when the polysilicon 14 forms sauce/drain diffused layer (not shown), it will be doped automatically, and is conductor-ized as a result. Although the polysilicon 14 may differ in the type and concentration of a dopant from the tungsten silicide 13 at this time, Since diffusion of the impurity in a thickness direction is suppressed with the thin tungsten nitride film 20 which intervenes among both, the work function of the interface part of the gate oxide 12 and the tungsten silicide 13 is maintained by the value as specified beforehand.

[0039]next, manufacturing method ****** explanation of the semiconductor device which has a gate electrode concerning this invention -- it carries out. Here, order is explained later on about the manufacturing method of the semiconductor device which has a gate electrode of the structure shown in drawing 2, referring to drawing 4 - drawing 13. However, numerals other than the numerals of explanation used by drawing 2 for convenience are used. First, as shown in drawing 4, on the silicon substrate 30, LOCOS process is used and the isolation region 31 is formed. Although not illustrated, if it is a case where a substrate is n type silicon, for example, a p type well will be formed as a field for creating a nMOS transistor. On the silicon substrate 30, the gate oxide 32 which consists of SiO_2 is formed.

[0040]Next, the tungsten silicide 33 is formed on the gate oxide 32. Membranous thickness is about 30 nm. In the stage film formation of this tungsten silicide 33 that forms membranes directly on the gate oxide 32. The tungsten silicide 33 is made into Si Rich (in WSi_x, it is x= 3 or more desirably) using the CVD method (dichlorosilane reduction CVD method) using the

mixed gas which contains tungsten hexafluoride (WF_6) and dichlorosilane (SiH_2Cl_2) as mentioned above. Thereby, the adhesion over the gate oxide 32 of the tungsten silicide 33 can be raised as mentioned above. Using Cold-Wall type LP gas-CVD system, the film formation condition at this time is a with the temperature of 680 **, and a pressure of 40 Pa basis, and passes SiH_2Cl_2, WF_6, and Ar by the flow of 160sccm, 1.6sccm, and 100sccm as reactant gas, respectively.

[0041]Then, the polysilicon 34 is formed. Membranous thickness is about 120 nm. Using Hot-Wall type LP gas-CVD system, the film formation condition at this time is a with the temperature of 625 **, and a pressure of 20 Pa basis, and passes SiH_4 by the flow of 400sccm as reactant gas. Drawing 5 shows the state where the tungsten silicide 33 and the polysilicon 34 were formed on the gate oxide 32. These two layers serve as a gate electrode like the after-mentioned. Next, as shown in drawing 6, the ion implantation of impurity ion is performed. This process is performed in order to conductor-ize the polysilicon 34 used as a gate electrode. The ion implantation of this is carried out by dose abbreviation $5x10^{15}$/accelerating voltage 15keV and cm^2, using phosphorus (P) as an impurity. The polysilicon 34 serves as a conductor mostly by this.

[0042]Then, the SiO_2 film 35 for forming stopper SiO_2 on the polysilicon 34 is formed. Drawing 7 shows the state where the SiO_2 film 35 was formed. Thickness makes it this stage film formation with about 150 nm for example, using an ordinary pressure CVD method. Next, as shown in drawing 8, on the SiO_2 film 35, resist is applied, it patterns based on the final shape of a gate electrode by a photolithography, and the resist mask 36 is formed. And etching processing of the SiO_2 is carried out based on this resist mask 36. This etching processing is performed, for example using a magnetron type etcher, passing CHF_3 by the flow of 45sccm as reactant gas under the conditions of the temperature of 20 **, the pressure of 2.7 Pa, and RF output 1000W. If the resist mask 36 is removed after that, as shown in drawing 9, the SiO_2 film 35a patternized by the shape of the gate electrode will be obtained.

[0043]Then, the polysilicon 34 and the tungsten silicide 33 are etched by using the patternized SiO_2 film 35a which was shown in drawing 9 as a mask. This etching processing is performed, for example using ECR plasma etcher by a with the temperature of 20 **, and a pressure of 0.4 Pa basis, and an RF output is set to 80W at the 1st step, and sets it to 30W at the 2nd step. It passes by the flow of 75sccm and 5sccm, respectively, using Cl_2 and O_2 for example as reactant gas. By this, as shown in drawing 10, the polysilicon 34a and the tungsten silicide 33a of the same pattern as the SiO_2 film 35a are obtained, and these serve as the gate electrode

37.

[0044]Next, the impurity to a LDD layer (not shown) is introduced. In this case, ion is had good control of striking in any direction with a resist mask to each of the nMOS transistor and pMOS transistor of CMOS. By providing a LDD layer, the electric field in the depletion layer in a drain end can weaken, and a hot electron effect can be inhibited. After introducing an impurity to a LDD layer, the sidewall 38 is formed in the side of the gate electrode 37 as shown in drawing 11. The purpose of forming the sidewall 38 is for preventing injecting the impurity into the lower layer LDD layer of the sidewall 38, when mainly forming sauce/drain diffused layer. In addition, about tungsten silicide, an oxidizing atmosphere will not be direct used by surrounding thoroughly high-melting point metal silicide, such as tungsten silicide, by the sidewall of polysilicon. For this reason, when the characteristic in the whole gate electrode to be oxidized improves and it forms an HTO film as a result, even if a gate electrode is exposed to an oxidizing atmosphere, the catastrophic oxidation of tungsten silicide is prevented and can control degradation of surface morphology (Morphology). The sidewall 38 deposits polysilicon on the whole surface first, and is formed by carrying out etchback by anisotropic etching processing after that.

[0045]Then, sauce/drain diffused layer is formed by carrying out the ion implantation of the impurity. At this time, as shown in drawing 12, in forming the pMOS transistor of CMOS and forming a nMOS transistor for example, for difluoride boron (BF_2) ion, it carries out the ion implantation for example, of the arsenic (As) ion. In this case, when you pour an impurity into one side among a nMOS transistor and a pMOS transistor, by carrying out the mask of the upper part of another side by the photoresist 39, each ion is had good control of striking in any direction, and let each be a predetermined conductivity type. The photoresist 39 is removed in the stage which became unnecessary.

[0046]If formation of above each class finishes, heat treatment for activating impurities, such as the gate electrode 37 which introduced the impurity, a LDD layer, sauce/drain diffused layer, will be performed. For example temperature shall be 1000 **, they make processing time 10 seconds, and the conditions at that time perform RTA (RapidThermal Annealing) processing in Ar atmosphere. As the usual process shows to drawing 13 after that, deposition of the interlayer insulation film 40, Formation of the contact hole 41, stopgap of the contact hole by the metal 42, formation of the wiring 43, etc. are performed one by one, and the CMOS device which has the LDD layer of structure and the sidewall of a gate electrode which are shown in drawing 2 is completed.

[0047]What is necessary is just to skip the process of forming stopper $SiO_2$35a among the manufacturing methods explained in the top, the process of forming a LDD layer, and the process of forming the sidewall 38 in the case of the CMOS device which has a gate electrode of the structure shown in drawing 1. In the case of the CMOS device which, on the other hand,

has a gate electrode of the structure shown in drawing 3, Before forming the polysilicon 34 after forming the tungsten silicide 33 shown by the upper drawing 5, about 3-nm tungsten nitride (WN_x) film 20 shown in drawing 3 can be obtained by performing processing [nitriding / the tungsten silicide 33 / processing / directly]. For example in NH_3 atmosphere, temperature shall be 850 **, it makes processing time 60 seconds, and the processing condition at this time performs RTA processing.

[0048]By inserting the tungsten nitride film 20 as shown in drawing 3 between the tungsten silicide 13 and the polysilicon 14, Unless the impurity ion at the time of forming sauce/drain diffused layer is poured even into the tungsten silicide 13, it can prevent that the impurity by the side of the polysilicon 14 is spread to the tungsten silicide 13 side with the tungsten nitride film 20. For this reason, the work function of the tungsten silicide 13 can be effectively prevented from changing by diffusion of an impurity.

[0049]Above, as explained in connection with drawing 6, it conductor-ized by doping phosphorus (P) to the polysilicon 34 of the upper layer of the gate electrode 37, but this may be other impurities (As), for example, arsenic, and boron (B). Above, as explained in connection with drawing 5, although the thickness of 120 nm and the sidewall 38 was 150 nm the thickness of 30 nm and the upper polysilicon silicon 34a, the thickness of the lower layer tungsten silicide 33a of the gate electrode 37, What these should be suitably changed for according to the performance of a request of each device, the purpose, the characteristic, etc. cannot be overemphasized. Although explained above taking the case of the CMOS device formed on what is called a bulk silicon substrate, this invention is applicable also to the CMOS device of SOI structure.

[0050]Although the case where tungsten silicide (WSi_x) was used as high-melting point metal silicide was explained above, Like other high-melting point metal silicide ($MoSi_x$), for example, molybdenum silicide, tantalum silicide ($TaSi_x$), and titanium silicides ($TiSi_x$), The effect that it is the same even when the lower layer portion of a gate electrode is formed using what does not react to the SiO_2 film used as a ground, Namely, a proper work function, symmetrization of threshold voltage V_{th} of the pMOS transistor and nMOS transistor of CMOS, The effect of mitigation of the tensile stress impressed to the reservation and gate oxide of the thickness of a grade which can prevent that impurity ion unnecessary for a channel part is poured in in the case of the diffusion-zone formation by adhesion with gate oxide and self align is acquired.

[0051]

[Effect of the Invention]As explained above, according to this invention, by making into high-melting point metal silicide the lower layer which touches gate oxide among gate electrodes, the work function which affects threshold voltage can be controlled near the center of the band

gap of silicon, and threshold voltage can be controlled to a proper value. Since the whole gate electrode can be made into sufficient thickness by forming comparatively small polysilicon of internal stress on this high-melting point metal silicide, When forming the sauce/drain diffused layer by self align, impurity ion can be effectively prevented from being injected into the channel part directly under a gate. Since the tensile stress impressed to gate oxide on the other hand since the thickness of high-melting point metal silicide with large internal stress can be formed in sufficient thinness becomes small and increase of leakage current or phase boundary charge is suppressed as a result, the reliability of a device can be improved. Since the work function near an interface with the oxide film of a gate electrode and sizes, such as thickness of a gate electrode, which affect threshold voltage can be designed independently, the degree of process option increases. Since high-melting point metal silicide will not be direct made into an oxidizing atmosphere by surrounding high-melting point metal silicide by the sidewall of polysilicon, Even if the characteristic of the whole gate electrode to be oxidized improves and a gate electrode is exposed to an oxidizing atmosphere as a result, the catastrophic oxidation of high-melting point metal silicide is prevented, and degradation of surface morphology (Morphology) can be controlled.

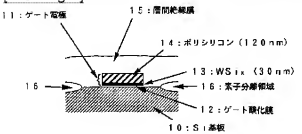
[Translation done.]

* NOTICES *

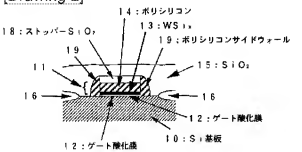
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

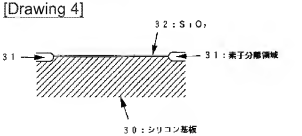
[Drawing 1]



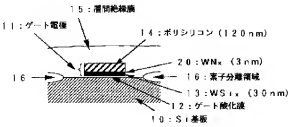
[Drawing 2]



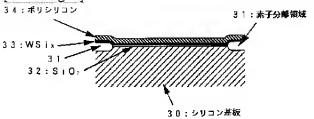
[Drawing 4]



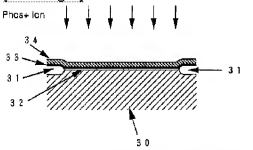
[Drawing 3]



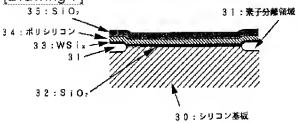
[Drawing 5]



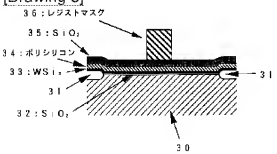
[Drawing 6]



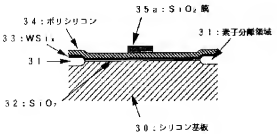
[Drawing 7]



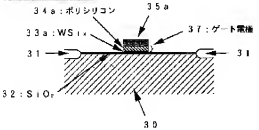
[Drawing 8]



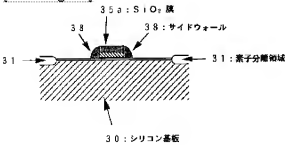
[Drawing 9]



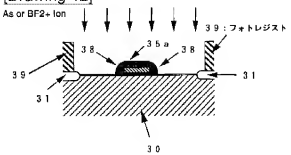
[Drawing 10]



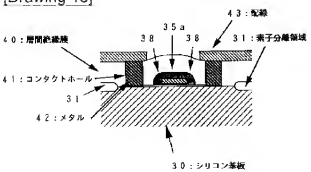
[Drawing 11]



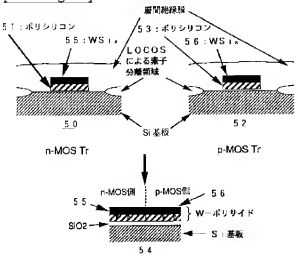
[Drawing 12]



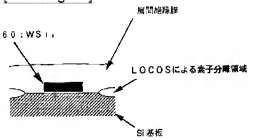
[Drawing 13]



[Drawing 14]



[Drawing 15]



[Translation done.]